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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Docket No. 93-C-07C2
Examiner: T. Cunningham
Art Unit: 2504

REQUEST FOR FILE WRAPPER CONTINUING APPLICATION UNDER 37 CFR 1.62

Box: FWC
HONORABLE COMMISSIONER OF
PATENTS AND TRADEMARKS
WASHINGTON, D.C. 20231

SIR: This is a request for filing a _____ continuation-in-part X continuation _____
divisional application under 37 CFR 1.62, of prior application serial no. 08/606,232 filed on February 23,
1996, entitled *DIRECT CURRENT SUM BANDGAP VOLTAGE COMPARATOR* by the following named
inventor(s).

Full Name of Inventor: William Carl Slemmer
Residence Address: 9114 Arborside Drive
City, County, State Dallas, Dallas County, Texas 75423
Citizenship: U.S.A.
Post Office Address: Same as Residence

The above identified prior application in which no payment of the issue fee, abandonment of, or
termination of proceedings has occurred, is hereby expressly abandoned as of the filing date of this new
application. Please use all the contents of the prior application file wrapper, including the drawings, as
the basic papers for the new application. (Note: 37 CFR 1.60 may be used for applications where the
prior application is not to be abandoned.)

1. _____ Enter the amendment previously filed on * under 37 CFR 1.116 but unentered, in the
prior application.
2. X A preliminary amendment is enclosed.
3. XX The filing fee is calculated on the basis of the claims existing in the prior application
as amended at 1 and 2 above.

Basic Fee		\$770.00
Extra Total Claims (____ x \$22.00)	=	
Extra Independent Claims (____ x \$80.00)	=	
Total Filing Fee:	=	\$770.00

Certificate of Mailing Under 37 C.F.R. § 1.18(a)

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sufficient postage as First Class Mail in an envelope addressed to: Assistant Commissioner of
Patents, Washington, D.C. 20231 on September 15, 1997.

by _____

Carolyn Wright

4. XX The Commissioner is hereby authorized to charge any fees under 37 CFR 1.16 and 1.17 which may be required, or credit any overpayment to Account No. 06-0580.
5. XX A check in the amount of \$770.00 is enclosed.
6. A new oath or declaration is included since this application is a continuation-in-part which discloses and claims additional matter.
7. XX Amend the specification by inserting before the first line of the following sentence:
- This is a Continuation-in-part, XX continuation, Division, of application serial no. 08/606,233, filed February 23, 1996.
8. A verified statement claiming small entity status is enclosed, (necessary even if a statement was filed in the prior application).
9. Priority of application serial no. *, filed on *, in * is claimed under 35 U.S.C.119.
10. XX The prior application is assigned of record to SGS-Thomson Microelectronics, Inc.
11. XX The power of attorney in the prior application is to Richard Robinson, Reg. No. 28,109 and Lisa K. Jorgenson, Reg. No. 34,845.
12. XX Address all future communications to: Lisa K. Jorgenson, SGS-Thomson Microelectronics, Inc., 1310 Electronics Drive, M/S 2346, Carrollton, Texas 75006.
13. Also enclosed: *

It is understood that secrecy under 35 U.S.C. 122 is hereby waived to the extent that if information or access is available to any one of the applications in the file wrapper of a 37 CFR 1.62 application, be it either this application or a prior application in the same file wrapper, the Patent and Trademark Office may provide similar information or access to all the other application in the same file wrapper.

9-15-97

(Date)



(Signature)

Address of signature

Dan Venglarik
Felsman, Bradley,
Gunter & Dillon, LLP
2600 Continental Plaza
777 Main Street
Fort Worth, Texas 76102

 Inventor(s)
 Assignee of complete interest
 Attorney or agent of record
 X Filed under Section 1.34(a)

09/18/97

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
W. SLEMMER

Serial No. 08/606,233

Filed: FEBRUARY 23, 1996

For: DIRECT CURRENT SUM
BANDGAP VOLTAGE
COMPARATOR

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Group Art Unit: 2504

Examiner: Cunningham, T.

Attorney Dkt. No.: 93-C-07C1

Certificate of Mailing Under 37 C.F.R. § 1.8(a)

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By:

Carolyn Wright

TRANSMITTAL LETTER

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Enclosed please find:

- Rule 1.62 Continuation Application;
- Preliminary Amendment;
- Petition for Extension of Time Within the Second Month;
- Amendment Under 37 C.F.R. § 1.116;
- Our checks for \$770.00 for the filing fee and \$390.00 for the extension fee; and
- Our return postcard which we would appreciate your date stamping and returning to us upon receipt.

DATE:

9-15-97

Respectfully submitted,

Don Venglarik

Dan Venglarik *Du*
Reg. No. 39,409
FELSMAN, BRADLEY, GUNTER
& DILLON, LLP
2600 Continental Plaza
777 Main Street
Fort Worth, TX 76102
(817) 332-8143

ATTORNEY FOR APPLICANT

exl. Sent to group 2504

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
W. SLEMMER

Serial No.

Filed: HEREWITH

For: DIRECT CURRENT SUM
BANDGAP VOLTAGE
COMPARATOR

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§ Group Art Unit:
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§ Examiner:
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§ Attorney Dkt. No.: 93-C-07C2
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Certificate of Mailing Under 37 C.F.R. § 1.8(a)

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By: _____

Carolyn Wright
Carolyn Wright

PRELIMINARY AMENDMENT

Box: FWC
Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

Prior to examination of the above-identified continuation application, please amend the application as follows. A check for the required fees is enclosed.

IN THE CLAIMS:

Please cancel claims 1, 4-14, 17-26 and 30.

Please amend the claims as follows:

1 27. (twice amended) A direct current sum bandgap voltage
2 comparator comprising:

3 a power supply having a predetermined threshold voltage
4 level which defines the minimum acceptable voltage level of the
5 power supply;

6 a summing node;

7 a plurality of current sources connected to the summing node
8 and directly connected to a power supply voltage, each current
9 source further comprising at least one field effect transistor
10 and at least one bipolar junction transistor and each current

11 source supplying a current to the summing node; and
12 an indicator circuit having an input connected to the
13 summing node, wherein the indicator circuit is responsive to
14 changes in the summing node voltage level and generates at an
15 output a logical signal at one state when the summing node
16 voltage level is greater than the predetermined threshold voltage
17 level and generates the logical signal at the output at another
18 state when the summing node voltage level is less than the
19 predetermined threshold voltage level.

Please add the following new claims:

1 --31. A direct current sum bandgap voltage comparator
2 comprising:

3 a summing node;

4 first and second current sources connected between the
5 summing node and a lower power supply; and

6 third and fourth current sources connected between the
7 summing node and an upper power supply,

8 wherein a voltage at the summing node equals a voltage of
9 the upper power supply when a current from the first and second
10 current sources to the summing node exceeds a current from the
11 third and fourth current sources to the summing node, and

12 wherein the voltage at the summing node equals a voltage of
13 the lower power supply when the current from the third and fourth
14 current sources to the summing node exceeds the current from the
15 first and second current sources to the summing node.

1 32. The direct current sum bandgap voltage comparator of claim
2 31, wherein the first current source further comprises:

3 a first field effect transistor connected between the lower
4 power supply and the summing node;

5 a second field effect transistor connected at a source to
6 the lower power supply and connected at a gate to a gate of the
7 first field effect transistor and a drain of the second field
8 effect transistor;

9 a third field effect transistor connected at a source to the

10 lower power supply and connected at a gate to the gate of the
11 first field effect transistor;

12 a fourth field effect transistors connected at a drain to
13 the drain of the second field effect transistor;

14 a fifth field effect transistor connected at a drain to a
15 drain of the third field effect transistor and to a gate of the
16 fifth field effect transistor and connected at the gate to a gate
17 of the fourth field effect transistor;

18 a first bipolar junction transistor connected at a base and
19 a collector to the upper power supply;

20 a second bipolar junction transistor connected at a base and
21 a collector to the upper power supply and connected at an emitter
22 to a source of the fifth field effect transistor; and

23 a resistor connected to an emitter of the first bipolar
24 junction transistor and to a source of the fourth field effect
25 transistor.

1 33. The direct current sum bandgap voltage comparator of claim
2 32, wherein the first, second, and third field effect transistors
3 are n-channel MOSFETs and the fourth and fifth field effect
4 transistors are p-channel MOSFETs.

1 34. The direct current sum bandgap voltage comparator of claim
2 32, wherein the first field effect transistor is sized to
3 generate a current of N times a current flowing through the
4 second field effect transistor.

1 35. The direct current sum bandgap voltage comparator of claim
2 31, wherein the first current source further comprises:

3 a current mirror including a field effect transistor
4 connected between the lower power supply and the summing node,
5 wherein the field effect transistor is sized to generate a
6 current of N times a current flowing through a portion of the
7 current mirror.

1 36. The direct current sum bandgap voltage comparator of claim
2 31, wherein the second current source further comprises:

3 a first field effect transistor connected between the lower
4 power supply and the summing node;

5 a second field effect transistor connected at a source to
6 the lower power supply and connected at a gate to a gate of the
7 first field effect transistor and a drain of the second field
8 effect transistor;

9 a third field effect transistor connected at a source to the
10 lower power supply and connected at a gate to the gate of the
11 first field effect transistor;

12 a fourth field effect transistor connected at a drain to the
13 drain of the second field effect transistor;

14 a fifth field effect transistor connected at a drain to a
15 drain of the third field effect transistor and to a gate of the
16 fifth field effect transistor and connected at the gate to a gate
17 of the fourth field effect transistor;

18 a bipolar junction transistor connected at a base and a
19 collector to the upper power supply and at an emitter to the
20 source of the fifth field effect transistor; and

21 a resistor connected between a source of the fourth field
22 effect transistor and the upper power supply.

1 37. The direct current sum bandgap voltage comparator of claim
2 36, wherein the first, second, and third field effect transistors
3 are n-channel MOSFETs and the fourth and fifth field effect
4 transistors are p-channel MOSFETs.

1 38. The direct current sum bandgap voltage comparator of claim
2 31, wherein the third current source further comprises:

3 a first field effect transistor connected between the upper
4 power supply and the summing node;

5 a second field effect transistor connected at a source to
6 the upper power supply and connected at a gate to a gate of the
7 first field effect transistor and a drain of the second field
8 effect transistor;

9 a third field effect transistor connected at a source to the
10 lower power supply and connected at a drain to the drain of the
11 second field effect transistor;

12 a fourth field effect transistor connected at a source to
13 the lower power supply, at a gate to a gate of the third field
14 effect transistor, and at a drain to the gate of the fourth field
15 effect transistor;

16 a fifth field effect transistor connected at a source to the
17 lower power supply;

18 a sixth field effect transistor connected at a drain to the
19 drain of the fourth field effect transistor;

20 a seventh field effect transistor connected at a drain to
21 a drain of the fifth field effect transistor and to a gate of the
22 seventh field effect transistor and connected at the gate to a
23 gate of the sixth field effect transistor;

24 an eighth field effect transistor connected at a drain and
25 at a gate to a source of the seventh field effect transistor and
26 at a source to the upper power supply; and

27 a resistor connected between a source of the sixth field
28 effect transistor and the upper power supply.

39. The direct current sum bandgap voltage comparator of claim
38, wherein the first, second, sixth, seventh, and eighth field
effect transistors are p-channel MOSFETs and the third, fourth
and fifth field effect transistors are n-channel MOSFETs.

40. The direct current sum bandgap voltage comparator of claim
31, wherein the fourth current source further comprises:

a first field effect transistor connected between the upper
power supply and the summing node;

a second field effect transistor connected at a source to
the upper power supply and connected at a gate to a gate of the
first field effect transistor and a drain of the second field
effect transistor; and

a resistor connected between a drain of the second field
effect transistor and the lower power supply.

41. The direct current sum bandgap voltage comparator of claim
40, wherein the first and second field effect transistors are p-
channel MOSFETs.

1 42. The direct current sum bandgap voltage comparator of claim
2 31, further comprising:
3 a cascode stage connected to the summing node.

1 43. The direct current sum bandgap voltage comparator of claim
2 31, further comprising:
3 a clamping circuit connected to the summing node.

1 44. The direct current sum bandgap voltage comparator of claim
2 31, further comprising:
3 a plurality of inverters connected in series between the
4 summing node and an output node.

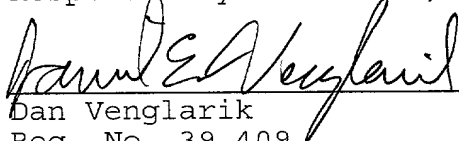
1 45. The direct current sum bandgap voltage comparator of claim
2 31, further comprising:
3 a hysteresis circuit connected to the output node and to the
4 fourth current source.--

REMARKS

Claims 27, 29, and 31-45 are pending in the present application. Claims 1, 4-14, 17-26, and 30 were canceled. Examination of the application is respectfully requested.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

Respectfully submitted,


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ATTORNEY FOR APPLICANTS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
W. SLEMMER

Serial No. 08/606,233

Filed: FEBRUARY 23, 1996

For: DIRECT CURRENT SUM
BANDGAP VOLTAGE
COMPARATOR

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§ Group Art Unit: 2504
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§ Examiner: Cunningham, T.
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§ Attorney Dkt. No.: 93-C-07C1
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By: _____

Carolyn Wright

AMENDMENT UNDER 37 C.F.R. § 1.116

Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

A two month extension of time is believed to be required. An appropriate petition and fee are enclosed. No additional fees are believed to be necessary; however, in the event that any additional fees are required for the prosecution of this application, please charge any necessary fees to Deposit Account No. 06-0580. No additional extension of time is believed to be necessary. If, however, an additional extension of time is needed, the extension is requested and please charge the fee for this extension to Deposit Account No. 06-0580.

In response to the Office Action dated January 15, 1997, please amend the above-identified application as follows:

IN THE CLAIMS:

Please cancel claims 27 and 29.

REMARKS

The application has been amended to cancel all claims not indicated to be allowable in the Office Action dated 01/15/97

(Paper No. 16).

It is respectfully urged that the subject application is now in condition for allowance. The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

Respectfully submitted,

Date: September 15, 1997



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